What is claimed is:

1. A memory cell, comprising:

a first transistor having a gate;

a second transistor having a gate;

the second transistor gate forming a load resistor for the first transistor such that the first transistor and the second transistor gate are coupled in series; and

the first transistor gate forming a load resistor for the second transistor such that the second transistor and the first transistor gate are coupled in series.

2. The memory cell of claim 1, wherein:

the first transistor is coupled to a power supply line with a constant potential and the second transistor gate is coupled to a ground reference line; and

the second transistor is coupled to a word reference line with an adjustable potential and the first transistor gate is coupled to a bit line power supply line with an adjustable potential.

3. The memory cell of claim 1, wherein:

the first transistor is a PMOS transistor with a polysilicon gate;

the second transistor is a NMOS transistor with a polysilicon gate;

the PMOS transistor is coupled between a first power supply line and the polysilicon gate of the NMOS transistor;

the polysilicon gate of the NMOS transistor is coupled between the PMOS transistor and a first reference line;

the polysilicon gate of the PMOS transistor is coupled between a second power supply line and the NMOS transistor; and

the NMOS transistor is coupled between the polysilicon gate of the PMOS transistor and a second reference potential line.

4. The memory cell of claim 1, wherein the first transistor and the second transistor form a bistable circuit such that a first stable state occurs when both the first transistor and the second transistor are on and a second stable state occurs when both the first transistor and the second transistor are off.

5. The memory cell of claim 1, wherein the first transistor gate and the second transistor gate are formed from a lightly doped polysilicon material.

6. A memory cell, comprising:

a first transistor having a gate;

a second transistor having a gate;

the second transistor gate forming a load resistor for the first transistor such that the first transistor and the second transistor gate are coupled in series, the first transistor being coupled to a power supply line with a constant potential and the second transistor gate being coupled to a ground reference line; and

the first transistor gate forming a load resistor for the second transistor such that the second transistor and the second transistor gate are coupled in series, the second transistor being coupled to a word reference line with an adjustable potential and the first transistor gate being coupled to a bit line power supply line with an adjustable potential.

7. The memory cell of claim 6, wherein the first transistor and the second transistor form a bistable circuit such that a first stable state occurs when both the first transistor and the second transistor are on and a second stable state occurs when both the first transistor and the second transistor are off.

8. The memory cell of claim 6, wherein the first transistor gate and the second transistor gate are formed from a lightly doped polysilicon material.

9. A two transistor SRAM cell, comprising:

a merged two transistor structure including two transistors, each transistor having a gate that functions as a load resistor for the other transistor;

a first node coupling the merged two transistor structure to a power supply line with a constant potential;

a second node coupling the merged two transistor structure to a first reference line with a constant potential;

a third node coupling the merged two transistor structure to a second power supply line with an adjustable potential; and

a fourth node coupling the merged two transistor structure to a second reference line with an adjustable potential.

10. The two transistor SRAM cell of claim 9, wherein the merged two transistor structure includes a PMOS transistor and a NMOS transistor operably coupled together to provide a bistable circuit such that a first stable state occurs when both the PMOS transistor and the NMOS transistor are on and a second stable state occurs when both the PMOS transistor and the NMOS transistor are off.

11. The two transistor SRAM cell of claim 9, wherein:

the merged two transistor structure includes a PMOS transistor with a gate and an NMOS transistor with a gate;

the PMOS transistor gate is connected in series with the NMOS transistor and functions as a pull-up load resistor; and

the NMOS transistor gate is connected in series with the PMOS transistor and functions as a pull-down load resistor.

12. The two transistor SRAM cell of claim 9, wherein:

the third node couples the merged two transistor structure to a column line; and

the fourth node couples the merged two transistor structure to a row line.

13. The two transistor SRAM cell of claim 9, wherein the gate of each transistor is formed from a lightly doped polysilicon material.

14. A two transistor SRAM cell, comprising:

a merged two transistor structure, including a PMOS transistor with a gate and an NMOS transistor with a gate such that the PMOS transistor gate is connected in series with the NMOS transistor and functions as a pull-up load resistor, and the NMOS transistor gate is connected in series with the PMOS transistor and functions as a pull-down load resistor;

a first node coupling the merged two transistor structure to a power supply line with a constant potential;

a second node coupling the merged two transistor structure to a first reference line with a constant potential;

a third node coupling the merged two transistor structure to a column line with an adjustable potential; and

a fourth node coupling the merged two transistor structure to a row line with an adjustable potential.

15. The two transistor SRAM cell of claim 14, wherein the PMOS transistor and the NMOS transistor are operably coupled together to provide a bistable circuit such that a first stable state occurs when both the PMOS transistor and the NMOS transistor are on and a second stable state occurs when both the PMOS transistor and the NMOS transistor are off.

16. The two transistor SRAM cell of claim 14, wherein the PMOS transistor gate and the NMOS transistor gate are formed from a lightly doped polysilicon material.

17. A merged structure SRAM cell, comprising:

a PMOS transistor having a first source/drain region, a second/source drain region, and a gate;

an NMOS transistor having a first source/drain region, a second source/drain region, and a gate; and

wherein:

the first source/drain region of the PMOS transistor is coupled to a PWRP power supply line;

the second source/drain region of the PMOS transistor is coupled to the gate of the NMOS transistor;

the gate of NMOS transistor is coupled to a first reference line such that the gate of the NMOS transistor forms a load resistor for the PMOS transistor;

the first source/drain region of the NMOS transistor is coupled to a second reference line;

the second source/drain region of the NMOS transistor is coupled to the gate of the PMOS transistor; and

the gate of the PMOS transistor is coupled to a PWRN power supply line such that the gate of the PMOS transistor forms a load resistor for the NMOS transistor.

18. The merged structure SRAM cell of claim 17, wherein the PMOS transistor and the NMOS transistor form a bistable circuit such that a first stable state occurs

when both the PMOS transistor and the NMOS transistor are on and a second stable state occurs when both the PMOS transistor and the NMOS transistor are off.

19. The merged structure SRAM cell of claim 17, wherein:

the PWRP power supply line has a constant potential;

the first reference line has a constant potential;

the PWRN power supply line is a bit line with an adjustable potential; and

the second reference line is a word reference line with an adjustable potential.

20. The merged structure SRAM cell of claim 17, wherein the PMOS transistor gate and the NMOS transistor gate are formed from a lightly doped polysilicon material.

21. A merged structure SRAM cell, comprising:

a PMOS transistor having a first source/drain region, a second/source drain region, and a gate;

an NMOS transistor having a first source/drain region, a second source/drain region, and a gate; and

wherein:

the first source/drain region of the PMOS transistor is coupled to a PWRP power supply line that has a constant potential;

the second source/drain region of the PMOS transistor is coupled to the gate of the NMOS transistor;

the gate of NMOS transistor is coupled to a first reference line that has a constant potential such that the gate of the NMOS transistor forms a load resistor for the PMOS transistor;

the first source/drain region of the NMOS transistor is coupled to a second reference line that has an adjustable potential;

the second source/drain region of the NMOS transistor is coupled to the gate of the PMOS transistor; and

the gate of the PMOS transistor is coupled to a PWRN power supply line that has an adjustable potential such that the gate of the PMOS transistor forms a load resistor for the NMOS transistor.

22. The merged structure SRAM cell of claim 21, wherein the PWRN power supply line is a column line and the second reference line is a row line.

23. The merged structure SRAM cell of claim 21, wherein the PMOS transistor gate and the NMOS transistor gate are formed from a lightly doped polysilicon material.

24. A memory system, comprising:

a plurality of memory cells, each including:

a first transistor having a gate;

a second transistor having a gate;

wherein the second transistor gate forms a load resistor for the first transistor such that the first transistor and the second transistor gate are coupled in series;

wherein the first transistor gate forms a load resistor for the second transistor such that the second transistor and the second transistor gate are coupled in series;

wherein the first transistor and the second transistor form a bistable circuit such that a first stable state occurs when both the first

transistor and the second transistor are on and a second stable state occurs when both the first transistor and the second transistor are off;

wherein a transition from the first state to the second state is slower than a transition from the second state to the first state; and

a plurality of sense amplifiers coupled to the plurality of memory cells, each including a predicted output circuit.

25. The memory system of claim 24, further including a processor in electrical communication with the plurality of memory cells and the sense amplifiers.

26. The memory system of claim 24, wherein the predicted output circuit is adapted for anticipating that the bistable circuit will be in the second state.

27. The memory system of claim 24, wherein:

the first transistor and second transistor gate are coupled in series between a power supply line that has a constant potential and a first reference line that has a constant potential;

the second transistor and first transistor gate are coupled in series between a column line that has an adjustable potential and a row line that has an adjustable potential; and

a cell state is determined by determining the current on the column line when the row line is stepped down to a lower potential.

28. The memory system of claim 24, wherein the first transistor gate and the second transistor gate are formed from a lightly doped polysilicon material.

29. A memory system, comprising:

a plurality of two-transistor SRAM cells, each including:

a merged two-transistor structure including two transistors, each transistor having a gate that functions as a load resistor for the other transistor;

a first node coupling the merged two transistor structure to a power supply line with a constant potential;

a second node coupling the merged two transistor structure to a first reference line with a constant potential;

a third node coupling the merged two transistor structure to a second power supply line with an adjustable potential;

a fourth node coupling the merged two transistor structure to a second reference line with an adjustable potential; and

wherein the merged two transistor structure includes a PMOS transistor and a NMOS transistor operably coupled together to provide a bistable circuit such that a first stable state occurs when both the PMOS transistor and the NMOS transistor are on and a second stable state occurs when both the PMOS transistor and the NMOS transistor are off; and

a plurality of sense amplifiers coupled to the plurality of two-transistor SRAM cells, each including a predicted output circuit.

30. The memory system of claim 29, further including a processor in electrical communication with the cell and the sense amplifier.

31. The memory system of claim 29, wherein the predicted output circuit is adapted for anticipating that the bistable circuit will be in the second state.

32. The memory system of claim 29, wherein each of the gates are formed from a lightly doped polysilicon material.

33. A memory system, comprising:

a plurality of merged structure SRAM cells, each including:

a PMOS transistor having a first source/drain region, a second/source drain region, and a gate;

an NMOS transistor having a first source/drain region, a second source/drain region, and a gate; and

wherein:

the first source/drain region of the PMOS transistor is coupled to a PWRP power supply line;

the second source/drain region of the PMOS transistor is coupled to the gate of the NMOS transistor;

the gate of NMOS transistor is coupled to a first reference line such that the gate of the NMOS transistor forms a load resistor for the PMOS transistor;

the first source/drain region of the NMOS transistor is coupled to a second reference line;

the second source/drain region of the NMOS transistor is coupled to the gate of the PMOS transistor;

the gate of the PMOS transistor is coupled to a PWRN power supply line such that the gate of the PMOS transistor forms a load resistor for the NMOS transistor; and

the PMOS transistor and the NMOS transistor form a bistable circuit such that a first stable state occurs when both the PMOS transistor and the NMOS transistor are on and a

second stable state occurs when both the PMOS transistor and the NMOS transistor are off; and

a plurality of sense amplifiers coupled to the plurality of merged structure SRAM cells, each including a predicted output circuit.

34. The memory system of claim 33, wherein the predicted output circuit is adapted for anticipating that the bistable circuit will be in the second state.

35. The memory system of claim 33, wherein the PMOS transistor gate and the NMOS transistor gate are formed from a lightly doped polysilicon material.

36. A SRAM circuit, comprising:

a SRAM memory array, including:

a plurality of memory cells, each including:

a first transistor having a gate;

a second transistor having a gate;

wherein the second transistor gate forms a load resistor for the first transistor such that the first transistor and the second transistor gate are coupled in series; and

wherein the first transistor gate forms a load resistor for the second transistor such that the second transistor and the second transistor gate are coupled in series;

a plurality of column lines, each being coupled to a column of memory cells; and

a plurality of row lines, each being coupled to a row of memory cells;

a row line voltage generator coupled to the plurality of row lines and adapted for selectively adjusting a row potential for one or more of the plurality of row lines;

a column line voltage generator coupled to the plurality of column lines and adapted for selectively adjusting a column potential for one or more of the plurality of column lines; and

a controller adapted for controlling the row line voltage generator and column line voltage generator.

37. The SRAM circuit of claim 36, wherein the first transistor gate and the second transistor gate are formed from a lightly doped polysilicon material.

38. The SRAM circuit of claim 36, wherein the first transistor and the second transistor form a bistable circuit such that a first stable state occurs when both the first transistor and the second transistor are on and a second stable state occurs when both the first transistor and the second transistor are off.

39. The SRAM circuit of claim 36, further including a column line current detector adapted for determining current flow in one or more of the column lines.

40. A SRAM circuit, comprising:

a SRAM memory array, including:

a plurality of memory cells, each including:

a merged two-transistor structure including two transistors, each transistor having a gate that functions as a load resistor for the other transistor;

a first node coupling the merged two transistor structure to a power supply line with a constant potential;

a second node coupling the merged two transistor structure to a first reference line with a constant potential;

a third node coupling the merged two transistor structure to a second power supply line with an adjustable potential; and

a fourth node coupling the merged two transistor structure to a second reference line with an adjustable potential;

a plurality of column lines, each being coupled to a column of memory cells;

a plurality of row lines, each being coupled to a row of memory cells;

a row line voltage generator coupled to the plurality of row lines and adapted for selectively adjusting a row potential for one or more of the plurality of row lines;

a column line voltage generator coupled to the plurality of column lines and adapted for selectively adjusting a column potential for one or more of the plurality of column lines; and

a controller adapted for controlling the row line voltage generator and column line voltage generator.

41. The SRAM circuit of claim 40, wherein each of the transistor gates are formed from a lightly doped polysilicon material.

42. The SRAM circuit of claim 40, wherein each merged two transistor structure includes a PMOS transistor and a NMOS transistor operably coupled together to provide a bistable circuit such that a first stable state occurs when both the PMOS transistor and the NMOS transistor are on and a second stable state occurs when both the PMOS transistor and the NMOS transistor are off.

43. The SRAM circuit of claim 40, further including a column line current detector adapted for determining current flow in one or more of the column lines.

44. A SRAM circuit, comprising:

a SRAM memory array, including:

a plurality of memory cells, each including:

a PMOS transistor having a first source/drain region, a second/source drain region, and a gate;

an NMOS transistor having a first source/drain region, a second source/drain region, and a gate; and

wherein:

the first source/drain region of the PMOS transistor is coupled to a PWRP power supply line;

the second source/drain region of the PMOS transistor is coupled to the gate of the NMOS transistor;

the gate of NMOS transistor is coupled to a first reference line such that the gate of the NMOS transistor forms a load resistor for the PMOS transistor;

the first source/drain region of the NMOS transistor is coupled to a second reference line;

the second source/drain region of the NMOS transistor is coupled to the gate of the PMOS transistor; and

the gate of the PMOS transistor is coupled to a PWRN power supply line such that the gate of the PMOS transistor forms a load resistor for the NMOS transistor;

a plurality of column lines, each being coupled to a column of memory cells; and

a plurality of row lines, each being coupled to a row of memory cells;

a row line voltage generator coupled to the plurality of row lines and adapted for selectively adjusting a row potential for one or more of the plurality of row lines;

a column line voltage generator coupled to the plurality of column lines and adapted for selectively adjusting a column potential for one or more of the plurality of column lines; and

a controller adapted for controlling the row line voltage generator and column line voltage generator.

45. The SRAM circuit of claim 44, wherein the PMOS transistor gate and the NMOS transistor gate are formed from a lightly doped polysilicon material.

46. A method of reading a memory cell, comprising:

applying a potential difference (V_{DIFF}) to a selected memory cell by providing a column potential (V_C) on a column line and a row potential (V_R) on a row line;

increasing V_{DIFF} by an increment less than a transistor threshold voltage (V_T); and

determining whether the increased V_{DIFF} results in a current flow on the column line for the selected memory cell.

47. The method of claim 46, wherein applying a potential difference (V_{DIFF}) to a selected memory cell includes applying V_C and V_R across a resistive load inverter in the selected memory cell.

48. The method of claim 47, wherein applying V_C and V_R across a resistive load inverter includes:

applying V_C and V_R across an NMOS resistive load inverter; and

increasing V_{DIFF} by an increment less than a transistor threshold voltage (V_T) includes:

maintaining a constant $V_{C;}$ and

decreasing V_R by an increment less than an NMOS transistor threshold voltage (V_{TN}).

49. The method of claim 46, wherein increasing V_{DIFF} by an increment less than a transistor threshold voltage V_T includes decreasing V_R by an increment less than a transistor threshold voltage V_T.

50. A method of writing a memory cell, comprising:

applying a potential difference (V_{DIFF}) to a selected memory cell by providing a column potential (V_C) on a column line and a row potential (V_R) on a row line; and

increasing V_{DIFF} by an increment more than a transistor threshold voltage (V_T) to set the selected memory cell to a one state.

51. The method of claim 50, wherein applying a potential difference (V_{DIFF}) to a selected memory cell includes applying V_C and V_R across a resistive load inverter in the selected memory cell.

52. The method of claim 51, wherein applying V_C and V_R across a resistive load inverter includes:

applying V_C and V_R across an NMOS resistive load inverter; and

increasing V_{DIFF} by an increment more than a transistor threshold voltage (V_T) includes:

maintaining a constant $V_{C;}$ and

decreasing V_R by an increment more than an NMOS transistor threshold voltage (V_{TN}).

53. The method of claim 50, wherein increasing V_{DIFF} by an increment more than a transistor threshold voltage V_T includes decreasing V_R by an increment more than a transistor threshold voltage V_T.

54. The method of claim 50, wherein decreasing V_{DIFF} by an increment more than V_T resets the selected memory cell to a zero state.

55. The method of claim 54, wherein decreasing V_{DIFF} by an increment more than V_T to reset the selected memory cell includes increasing V_R by an increment more than V_T.

56. A method of operating a memory array, comprising:

applying a potential difference (V_{DIFF}) to each of a plurality of memory cells by providing a column potential (V_C) on a column line and a row potential (V_R) on a row line;

resetting a first selected memory cell to a zero state by decreasing V_{DIFF} by an increment more than a transistor threshold voltage (V_T) to reset the selected memory cell to a zero state;

writing a second selected memory cell to a one state by increasing V_{DIFF} by an increment more than V_T to set the selected memory cell to the one state; and

reading a third selected memory cell by:

increasing V_{DIFF} by an increment less than V_T; and

determining whether the increased V_{DIFF} results in a current flow on the column line for the selected memory cell.

57. The method of claim 56, wherein applying a potential difference (V_{DIFF}) in each of a plurality of memory cells includes applying V_C and V_R across a resistive load inverter in each of the plurality of memory cells.

58. The method of claim 57, wherein:

applying V_C and V_R across a resistive load inverter includes applying V_C and V_R across an NMOS resistive load inverter; and

writing a second selected memory cell by increasing V_{DIFF} by an increment more than a transistor threshold voltage (V_T) includes:

maintaining a constant V_C; and

decreasing V_R by an increment more than an NMOS transistor threshold voltage (V_{TN}).

59. The method of claim 56, wherein writing a second selected memory cell by increasing V_{DIFF} by an increment more than a transistor threshold voltage V_T includes decreasing V_R by an increment more than a transistor threshold voltage V_T.

60. The method of claim 56, wherein resetting a first selected memory cell includes resetting a row of cells by adjusting V_R by an increment larger than V_T.

61. The method of claim 56, wherein writing a second selected memory cell to a one state by increasing V_{DIFF} by an increment more than V_T includes:

adjusting V_R for a write operation by an increment greater than a transistor threshold voltage to turn a first transistor on for cells within a selected row; and

adjusting a second column potential V_C on a second column line by an amount to prevent a second transistor in the selected row from turning on in response to adjusting the row potential for the write operation.

62. The method of claim 56, wherein reading a third selected memory cell includes:

decreasing V_R by an increment less than a transistor threshold voltage increment; and

determining if the decreased V_R results in a current flow on a corresponding column line for the memory cell.

63. A method of forming a memory cell, comprising:

forming a PMOS transistor with a gate;

forming an NMOS transistor with a gate;

coupling the PMOS transistor gate in series with the NMOS transistor; and

coupling the NMOS transistor gate in series with the PMOS transistor.

64. The method of claim 63, further including:

coupling the PMOS transistor and the NMOS transistor gate between a PWRP power supply and a first reference line; and

coupling the NMOS transistor and the PMOS transistor gate between a PWRN power supply and a second reference line.

65. The method of claim 63, further including:

coupling the PMOS transistor and the NMOS transistor gate between a constant power supply and a ground reference line; and

coupling the NMOS transistor and the PMOS transistor gate between a column line with an adjustable potential and a row line with an adjustable potential.

66. The method of claim 63, wherein forming a PMOS transistor with a gate and forming an NMOS transistor with a gate includes forming a lightly doped polysilicon gate for both the PMOS transistor and the NMOS transistor.

67. The method of claim 63, wherein coupling the PMOS transistor gate in series with the NMOS transistor and coupling the NMOS transistor gate in series with the PMOS transistor includes forming the NMOS transistor gate as a PMOS load resistor and forming the PMOS transistor gate as an NMOS load resistor.

68. A method of forming a memory system, comprising:

forming a memory cell, including:

forming a PMOS transistor with a gate;

forming an NMOS transistor with a gate;

coupling the PMOS transistor gate in series with the NMOS transistor; and

coupling the NMOS transistor gate in series with the PMOS transistor; and

forming a sense amplifier that includes a predicted output circuit for anticipating that the bistable circuit will be in the second state.

69. The method of claim 68, wherein forming a memory cell by forming a PMOS transistor with a gate and forming an NMOS transistor with a gate includes forming a lightly doped polysilicon gate for both the PMOS transistor and the NMOS transistor.

70. The method of claim 68, further including:

coupling the PMOS transistor and the NMOS transistor gate between a PWRP power supply and a first reference line; and

coupling the NMOS transistor and the PMOS transistor gate between a PWRN power supply and a second reference line.

71. The method of claim 68, further including:

coupling the PMOS transistor and the NMOS transistor gate between a constant power supply and a ground reference line; and

coupling the NMOS transistor and the PMOS transistor gate between a column line with an adjustable potential and a row line with an adjustable potential.

72. A method of forming a SRAM circuit, comprising:

providing a memory array, a controller, a row line voltage generator, a column line voltage generator, and a column line current detector;

coupling the controller to the row line voltage generator, the column line voltage generator, and the column line current detector;

coupling the row line voltage generator to row lines within the memory array such that the controller is able to vary a potential on a selected row line;

coupling the column line voltage generator to column lines within the memory array such that the controller is able to vary a potential on one or more selected column lines; and

coupling the column line current detector to the column lines within the memory array such that the controller is able to determine current flow on a selected current line.

73. The method of claim 71, wherein providing a memory array includes providing a plurality of memory cells, each cell being provided by:

forming a PMOS transistor with a gate;

forming an NMOS transistor with a gate;

coupling the PMOS transistor gate in series with the NMOS transistor; and

coupling the NMOS transistor gate in series with the PMOS transistor.

74. The method of claim 71, forming a memory cell by forming a PMOS transistor with a gate and forming an NMOS transistor with a gate includes forming

a lightly doped polysilicon gate for both the PMOS transistor and the NMOS transistor.

75. The method of claim 72, further including:

coupling the PMOS transistor and the NMOS transistor gate between a PWRP power supply and a first reference line; and

coupling the NMOS transistor and the PMOS transistor gate between a PWRN power supply and a second reference line.

76. The method of claim 71, further including:

coupling the PMOS transistor and the NMOS transistor gate between a constant power supply and a ground reference line; and

coupling the NMOS transistor and the PMOS transistor gate between a column line with an adjustable potential and a row line with an adjustable potential.